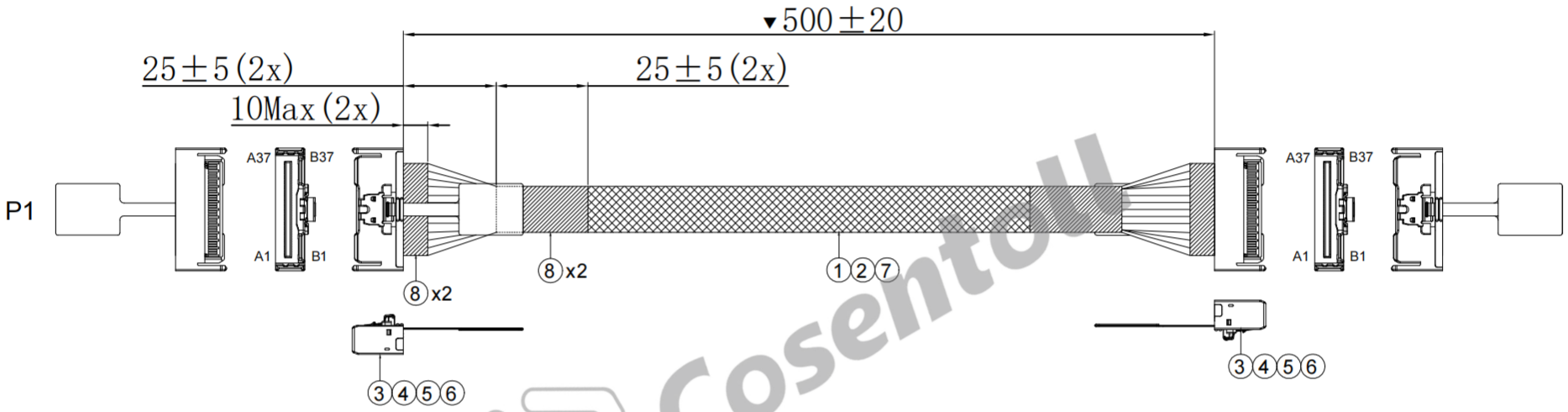
RoHS Complied HF

Revisions					
ECN No.	REV.	Descriptions	Checked	Approved	Date
	V1.0	NEW	Kevin	Mike	27/03/2023



NOTES:
1. THIS PRODUCT CONFORMS TO THE MECHANICAL DIMENSIONING REQUIREMENTS OF SFF-TA-1016.
2. THIS PRODUCT MEETS PCIe GEN5.
3. CABLE WELDING AREA IMPEDANCE: 85±15ohm.RAW CABLE IMPEDANCE: 85±10ohm.
4. DIMENSIONS MARKED" " SHALL BE CHECKED.
5.TEST CONDITION:
   a. 100% OPEN SHORT & MIS-WIRE TEST,
   b. CONDUCTIVE RESISITANCE:2Ω/MAX,
   c. INSULATION RESISTANCEI:10MΩ/MIN.AT DC 300V

序号	描述	数量	单位
8	ACETATE TAPE,BLACK,T=0.12MM,RoHS2.0	A/R	M
7	WEAVE.PET WEAVE Ø9.0MM BLACK VW-1,RoHS2.0	A/R	M
6	INNERMOLD,HOT MELT ADHESIVE,BLACK,UL94V-0,RoHS2.0	A/R	KG
5	LATCH,FOR MCIO 74PIN,SUS301,3/4H,T=0.25mm,WITH PULL-TAB,RoHS2.0	2	PCS
4	COVER,MCIO 8X ST COVER(COVER+BACK PLUG),BLACK,UL94V-0,RoHS2.0	2	SET
3	PCB FOR MCIO 8X ST,BASE METAL:COPPER,PLATING:Au(30u" Min) OVER Ni(100u" Min),85ohm,RoHS2.0	2	PCS
2	SAS CABLE, (32AWG*1P+32AWG*1D)*1P,TIN-PLATED COPPER,BLUE,RoHS2.0	A/R	M
1	SAS 5.0 CABLE,(30AWG*1P+34AWG*2D)*1P 85ohm,蓝色 反包	A/R	M

X	±1
XX	±0.5
XXX	±0.3
0-180°	±3°
UNITS	mm

Customer P/N: NA
Customer REV: A
Port No: 23032701

Cosentoll Technology Co., Ltd

TITLE: MCIO x8 to MCIO x8 L=500MM

APPD: Mike	Date: 27/03/2023	DWG NO: CST-MM701
CHKD: Kevin	Date: 27/03/2023	
DRAW: Eric	Date: 27/03/2023	

SCALE	SHEET	REV.
NONE	1/2	1.0

RoHS Complied HF

Revisions					
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WIRING TABLE

P1 —— P2

	MB	BP	
Signal	P1-VT X8 MCIO	P2-VT X8 MCIO	Signal
GND	A1	B1	GND
P5E_CPU0_PE0_RX_DN<0>	A2	B2	PCIE0_RX_DP<0>
P5E_CPU0_PE0_RX_DP<0>	A3	B3	PCIE0_RX_DN<0>
GND	A4	B4	GND
P5E_CPU0_PE0_RX_DN<1>	A5	B5	PCIE0_RX_DP<1>
P5E_CPU0_PE0_RX_DP<1>	A6	B6	PCIE0_RX_DN<1>
GND	A7	B7	GND
PE_MCIO0_BPTYPE_WAKE_N	A8	B8	PE_MCIO1_PORT1_BP_TYPE
FM_SMB_CPU0_ALERT_N	A9	B9	HP_ALERT
GND	A10	B10	GND
PCIE_MCIO0_CLK_PORT1_100M_DP	A11	B11	PCIE_CLK_0_100M_DP
PCIE_MCIO0_CLK_PORT1_100M_DN	A12	B12	PCIE_CLK_0_100M_DN
GND	A13	B13	GND
P5E_CPU0_PE0_RX_DN<2>	A14	B14	PCIE0_RX_DP<2>
P5E_CPU0_PE0_RX_DP<2>	A15	B15	PCIE0_RX_DN<2>
GND	A16	B16	GND
P5E_CPU0_PE0_RX_DN<3>	A17	B17	PCIE0_RX_DP<3>
P5E_CPU0_PE0_RX_DP<3>	A18	B18	PCIE0_RX_DN<3>
GND	A19	B19	GND
P5E_CPU0_PE0_RX_DN<4>	A20	B20	PCIE0_RX_DP<4>
P5E_CPU0_PE0_RX_DP<4>	A21	B21	PCIE0_RX_DN<4>
GND	A22	B22	GND
P5E_CPU0_PE0_RX_DN<5>	A23	B23	PCIE0_RX_DP<5>
P5E_CPU0_PE0_RX_DP<5>	A24	B24	PCIE0_RX_DN<5>
GND	A25	B25	GND
PE_MCIO0_PWRBRK_N	A26	B26	PE_MCIO1_PORT2_BP_TYPE
TP_MCIO0_SGPIO_LOAD	A27	B27	NC_I3_B27
GND	A28	B28	GND
PCIE_MCIO0_CLK_PORT2_100M_DP	A29	B29	PCIE_CLK_1_100M_DP
PCIE_MCIO0_CLK_PORT2_100M_DN	A30	B30	PCIE_CLK_1_100M_DN
GND	A31	B31	GND
P5E_CPU0_PE0_RX_DN<6>	A32	B32	PCIE0_RX_DP<6>
P5E_CPU0_PE0_RX_DP<6>	A33	B33	PCIE0_RX_DN<6>
GND	A34	B34	GND
P5E_CPU0_PE0_RX_DN<7>	A35	B35	PCIE0_RX_DP<7>
P5E_CPU0_PE0_RX_DP<7>	A36	B36	PCIE0_RX_DN<7>
GND	A37	B37	GND

P1 —— P2

	MB	BP	
Signal	P1-VT X8 MCIO	P2-VT X8 MCIO	Signal
GND	B1	A1	GND
P5E_CPU0_PE0_TX_DN<0>	B2	A2	PCIE0_TX_DN<0>
P5E_CPU0_PE0_TX_DP<0>	B3	A3	PCIE0_TX_DP<0>
GND	B4	A4	GND
P5E_CPU0_PE0_TX_DN<1>	B5	A5	PCIE0_TX_DN<1>
P5E_CPU0_PE0_TX_DP<1>	B6	A6	PCIE0_TX_DP<1>
GND	B7	A7	GND
SMB_PEHPCPU0_NVME0_1_LVC3_R_SCL	B8	A8	I2C_HP0_SCL
SMB_PEHPCPU0_NVME0_1_LVC3_R_SDA	B9	A9	I2C_HP0_SDA
NC_MCIO0_B10	B10	A10	MCIO1_MB_HBA_TYPE
PE_MCIO0_PCIE_RST_N	B11	A11	PE_MCIO1_PORT1_RST_N
PE_MCIO0_PCIE_BIF0	B12	A12	PE_MCIO_PCIE_BIF0
GND	B13	A13	GND
P5E_CPU0_PE0_TX_DN<2>	B14	A14	PCIE0_TX_DN<2>
P5E_CPU0_PE0_TX_DP<2>	B15	A15	PCIE0_TX_DP<2>
GND	B16	A16	GND
P5E_CPU0_PE0_TX_DN<3>	B17	A17	PCIE0_TX_DN<3>
P5E_CPU0_PE0_TX_DP<3>	B18	A18	PCIE0_TX_DP<3>
GND	B19	A19	GND
P5E_CPU0_PE0_TX_DN<4>	B20	A20	PCIE0_TX_DN<4>
P5E_CPU0_PE0_TX_DP<4>	B21	A21	PCIE0_TX_DP<4>
GND	B22	A22	GND
P5E_CPU0_PE0_TX_DN<5>	B23	A23	PCIE0_TX_DN<5>
P5E_CPU0_PE0_TX_DP<5>	B24	A24	PCIE0_TX_DP<5>
GND	B25	A25	GND
MCIO0_BMC_I2C_SCL	B26	A26	MCIO1_BMC_I2C_SCL
MCIO0_BMC_I2C_SDA	B27	A27	MCIO1_BMC_I2C_SDA
TP_MCIO0_SGPIO_CLK	B28	A28	GND
TP_MCIO0_SGPIO_DO	B29	A29	PE_MCIO1_PORT2_RST_N
PE_MCIO0_PCIE_BIF1	B30	A30	PE_MCIO_PCIE_BIF1
GND	B31	A31	GND
P5E_CPU0_PE0_TX_DN<6>	B32	A32	PCIE0_TX_DN<6>
P5E_CPU0_PE0_TX_DP<6>	B33	A33	PCIE0_TX_DP<6>
GND	B34	A34	GND
P5E_CPU0_PE0_TX_DN<7>	B35	A35	PCIE0_TX_DN<7>
P5E_CPU0_PE0_TX_DP<7>	B36	A36	PCIE0_TX_DP<7>
GND	B37	A37	GND

X	±1
XX	±0.5
XXX	±0.3
0-180°	±3°
UNITS	mm

Customer P/N: NA
Customer REV: A
Port No:

Cosentoll Technology Co., Ltd

TITLE: MCIO x8 to MCIO x8 L=500MM

APPD:	Mike	Date: 27/03/2023
CHKD:	Kevin	Date: 27/03/2023
DRAW:	Eric	Date: 27/03/2023

DWG NO: CST-MM701

SCALE	SHEET	REV.
NONE	2/2	1.0